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## **Amendments to the Claims:**

This listing of the claims replaces all prior versions, and listings, of the claims in the application.

## **Listing of Claims:**

1. (Previously Presented) An automated method for designing an integrated circuit (IC) design-specific cell, said method comprising the steps of:

receiving a design specification for electrical behavior or transistor-level characteristics of said design-specific cell;

mapping to a transistor-level representation of said design-specific cell, said mapping based on said design specification; and

evaluating said transistor-level representation of said design-specific cell for meeting said design specification.

- 2. (Previously Presented) The method of claim 1, wherein said step of evaluating comprises evaluating said transistor-level representation of said design-specific cell based on a specific design context in which said design-specific cell is to be used.
- 3. (Original) The method of claim 1, wherein said step of receiving comprises receiving a description of said design-specific cell.
- 4. (Original) The method of claim 3, wherein said description is selected from a group consisting of a netlist representation, a descriptive language representation, and a standard-cell representation of said design-specific cell, wherein said standard-cell is used in an IC design process.

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5. (Original) The method of claim 1, wherein said design specification is selected from the group consisting of: size (area), signal timing, transistor sizing, number of transistors, power consumption, length of interconnects within said design-specific cell, output signal strength, input signal impedance, noise characteristics, and a combination thereof.

6. (Original) The method of claim 1, wherein said step of mapping comprises:

generating a transistor netlist based on at least one netlist generation algorithm; and

evaluating said generated transistor netlist based on at least one design specification.

- 7. (Original) The method of claim 1, wherein said step of mapping is based on at least one of a plurality of topology formats.
- 8. (Original) The method of claim 6, wherein said step of mapping further comprises optimizing transistor size for said generated transistor netlist.
- 9. (Original) The method of claim 1, wherein said method further comprises the step of creating at least one transistor-level redundancy for aiding in satisfying said design specification.
- 10.(Original) The method of claim 1, wherein said method further comprises the step of detecting an implementation weakness in a cell for implementing said IC.
  - 11.(Previously Presented) A system for automatically designing an

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integrated circuit (IC) design-specific cell, said system comprising:

an interface for receiving a design specification for electrical behavior or transistor-level characteristics of said design-specific cell;

means for mapping a transistor-level representation of said design-specific cell, wherein said means for mapping uses said design-specific specification as a basis for the mapping; and

means for evaluating said transistor-level representation of said designspecific cell for determining whether said transistor-level representation of said IC meets said design specification.

- 12. (Previously Presented) The system of claim 11, wherein said means for evaluating is capable of evaluating said transistor-level representation of said design-specific cell based on a specific design context in which said design-specific cell is to be used.
- 13.(Original) The system of claim 11, wherein said interface receives a description of said design-specific cell.
- 14.(Original) The system of claim 13, wherein said description received by said interface is selected from a group consisting of: a netlist representation, a descriptive language representation, and a standard-cell representation of said design-specific cell, wherein said standard-cell is used in an IC design process.
- 15. (Original) The system of claim 11, wherein said means for mapping controls the mapping of said transistor-level representation on the basis of said design-specific specification selected from the group consisting of: size (area), signal timing, transistor sizing, number of transistors, power consumption,

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fault tolerance, integrity characteristics, noise characteristics, and a combination thereof.

- 16. (Original) The system of claim 11, wherein said means for mapping is capable of generating a transistor netlist based on at least one netlist generation algorithm; and evaluating said generated transistor netlist based on at least one design specification.
- 17. (Original) The system of claim 11, wherein said means for mapping further comprises a control means for the mapping using a plurality of topology formats.
- 18.(Original) The system of claim 11, wherein said means for mapping further comprises a control means for optimization of transistor sizing for said generated transistor netlist.
- 19. (Original) The system of claim 11, wherein said system further comprises means for creating at least one transistor-level redundancy for said IC cell for aiding in meeting said design specification.
- 20.(Original) The system of claim 11, wherein said system further comprises means for detecting an implementation weakness in a cell for implementing said IC. .
- 21. (Previously Presented) A design-specific cell produced by an automated integrated circuit (IC) design process, said IC design process comprises the steps of:

receiving a design specification for electrical behavior or transistor-level characteristics of said design-specific cell;

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mapping a transistor-level representation of said design-specific cell, said mapping based on said design specification; and

evaluating said transistor-level representation of said design-specific cell for meeting of said design specification.

- 22. (Previously Presented) The design-specific cell produced by the IC design process of claim 21, wherein said step of evaluating comprises evaluating said transistor-level representation of said design-specific cell based on a specific design context in which said design-specific cell is to be used.
- 23. (Original) The design-specific cell produced by the IC design process of claim 21, wherein said step of receiving comprises receiving a description of said design-specific cell.
- 24. (Original) The design-specific cell produced by the IC design process of claim 23, wherein said description is selected from a group consisting of: a netlist representation, a descriptive language representation, and a standard-cell representation of said design-specific cell, wherein said standard-cell is used in an IC design process.
- 25. (Original) The design-specific cell produced by the IC design process of claim 21, wherein said design specification is selected from the group consisting of: size (area), signal timing, transistor sizing, number of transistors, power consumption, length of interconnects within said design-specific cell, output signal strength, input signal impedance, noise characteristics, and a combination thereof.
- 26. (Original) The design-specific cell produced by the IC design process of claim 21, wherein said step of mapping comprises:

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generating a transistor netlist based on at least one netlist generation algorithm; and

evaluating said generated transistor netlist based on at least one design specification.

- 27.(Original) The design-specific cell produced by the IC design process of claim 21, wherein said step of mapping is based on at least one plurality of topology format.
- 28.(Original) The design-specific cell produced by the IC design process of claim 21, wherein said step of mapping further comprises means for optimizing the transistor size for said generated transistor netlist.
- 29.(Original) The design-specific cell produced by the IC design process of claim 21, wherein said method further comprises the step of creating at least one transistor-level redundancy for aiding in meeting said design specification.
- 30. (Previously Presented) A storage medium having computer readable program instructions embodied therein for automatically designing an integrated circuit (IC) design-specific cell, said storage medium comprising:

program instructions for receiving a design specification for electrical behavior or transistor-level characteristics of said design-specific cell;

program instructions for mapping a transistor-level representation of said design-specific cell, said mapping based on said design specification; and

program instructions for evaluating said transistor-level representation of said design-specific cell for satisfaction of said design specification.

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31. (Previously Presented) The method of claim 1, wherein said design specification comprises electrical behavior and transistor-level characteristics of said design-specific cell.

- 32. (Previously Presented) The system of claim 11, wherein said design specification comprises electrical behavior and transistor-level characteristics of said design-specific cell.
- 33. (Previously Presented) The design-specific cell produced by an automated integrated circuit (IC) design process of claim 21, wherein said design specification comprises electrical behavior and transistor-level characteristics of said design-specific cell.
- 34. (Previously Presented) The storage medium of claim 30, wherein said design specification comprises electrical behavior and transistor-level characteristics of said design-specific cell.
- 35. (New) The method of claim 1, wherein said integrated circuit design-specific cell is selected from the group consisting of: CMOS cells, static CMOS cells, dynamic CMOS cells and combinations thereof.
- 36.(New) The system of claim 11, wherein said integrated circuit design-specific cell is selected from the group consisting of: CMOS cells, static CMOS cells, dynamic CMOS cells and combinations thereof.
- 37.(New) The design-specific cell of claim 21, wherein the integrated circuit design-specific cell is selected from the group consisting of: CMOS cells, static CMOS cells, dynamic CMOS cells and combinations thereof.
  - 38.(New) The storage medium of claim 30, wherein said integrated

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circuit design-specific cell is selected from the group consisting of: CMOS cells, static CMOS cells, dynamic CMOS cells and combinations thereof.